IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: David J. Keller	§	
	§	GAU: 1763
Serial No.: 09/458,875	§	Examiner: George Goudreau
Filed: December 10, 1999	§	Atty. Docket: 99-0738.00
For: **POLYSILICON ETCH USEFUL DURING THE MANUFACTURE OF A SEMICONDUCTOR DEVICE**	§	Confirmation No.: 9389
	§	Paper No. 12

Box Non Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

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RESPONSE TO THE ELECTION REQUIRMENT OF JANUARY 2, 2003

Please enter the following in response to the Examiner's election requirment of January 2, 2003.

Election

Applicant elects the invention of Group I, claims 27-30, 33-36, without traverse. Accordingly, please cancel claims 31 and 32 without prejudice.

Preliminary Amendment

Prior to examining the above-captioned application, please add the following new claims 37 and 38 as set forth below.

-- 37. A method used to form an electronic device having a semiconductor device, the semiconductor device formed by a method comprising:

providing a semiconductor wafer substrate assembly having a planarized wafer surface and at least first and second features in spaced relation to each other which define a region comprising an opening between said first and second features;

forming a conductive layer over said first and second features and within said opening;

providing a patterned mask layer over said conductive layer, said patterned mask layer having an opening therein which exposes said region between said first and second features;

etching said conductive layer within said opening between said first and second features using a continuous etch comprising:

a first etch which erodes said conductive layer with ions traveling in a first direction substantially perpendicular with a plane of said planarized wafer surface and leaves conductive stringers between said first and second features subsequent to said first etch; then

a second etch which electrically charges said ions to bend said charged ions into said stringers in a second direction which is less perpendicular with said plane of said planarized wafer surface than said first direction and removes said conductive stringers remaining between said first and second features.

38. The method of claim 37 further comprising:

during said first etch:

introducing an oxygen-containing gas into a chamber at an oxygen flow rate of between about 1.9 sccm and about 2.7 sccm;

introducing a halogen-containing gas into said etch chamber at a halogen flow rate of between about 35 sccm to about 65 sccm; and

subjecting said semiconductor wafer substrate assembly to a top power of between about 245 watts to about 315 watts; and

during said second etch:

increasing said flow rate of said oxygen-containing gas to an oxygen flow rate of between about 3.6 sccm to about 4.7 sccm;

maintaining said halogen-containing gas flow rate at a halogen flow rate of between about 35 sccm to about 65 sccm; and

increasing said top power to between about 385 watts and about 455 watts. --